CIC Compiler

December 2006, Version 7.0 — Errata Sheet

This document addresses known errata and documentation issues for the Altera® CIC Compiler, v7.0. Errata are functional defects or errors, which may cause an Altera CIC Compiler MegaCore® function to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

Table 1 shows the issues that affect the CIC Compiler, v7.0.

Table 1. CIC Compiler, v7.0 Issues

For the most up-to-date errata for this release, refer to the errata sheet on the Altera website:

www.altera.com/literature/es/es_cic_70.pdf

CIC Compiler, v7.0 Issues

Altera has identified the following issue that affects the CIC Compiler, v7.0.

Top level Verilog HDL is Classified as VHDL

The top-level Verilog HDL file in the generated Tcl script for compilation in the Quartus II software is classified as VHDL_FILE.

Affected Configurations

This issue affects all configurations with a top level Verilog HDL file.

Design Impact

The CIC Compiler generates a Tcl script (<*variation name*>**_quartus.tcl**) which can be used to run compilation in the Quartus II software. All the files are listed in this script as VHDL_FILE.

For example:

```
set_global_assignment -name "VHDL_FILE" miso_dec_input.v
```

An error is issued if the Tcl script is used for compilation in the Quartus II software.

Workaround

Edit the TCL script and change the global assignment line to:

```
set_global_assignment -name "VERILOG_FILE" miso_dec_input.v
```

Solution Status

This issue will be fixed in a future release of the CIC Compiler.

NativeLink Does Not Pass v2k Argument to VCS for Verilog-2001

NativeLink does not pass the `v2k` argument to VCS when the analysis and synthesis setting for Verilog HDL Input is set to `Verilog-2001`.

Affected Configurations

This issue affects all configurations.

Design Impact

The following error is generated when performing RTL simulation using the generated Verilog HDL testbench and targeting the VCS simulation environment using NativeLink in the Quartus II software:

```
Error: VCS: Error-[V2KS] Verilog 2000 IEEE 1364-2000 syntax used.
Please compile with +v2k
Error: VCS: to support this construct
Error: VCS: operator '**' .
```

Workaround

In the generated Verilog HDL testbench **<***output name***>_tb.v**, replace the power of operators with the calculated value, and add a wire declaration for the `clken` port.

Solution Status

This issue will be fixed in a future release of the CIC Compiler.

Contact Information

For more information, contact Altera's mySupport website at **www.altera.com/mysupport** and click **Create New Service Request**. Choose the **Product Related Request** form.

Revision History

Table 2 shows the revision history for the *CIC Compiler v7.0 Errata Sheet*.

Table 2. CIC Compiler Compiler v7.0 Errata Sheet Revision History

Version	Date	Errata Summary
7.0	December 2006	First release of this errata sheet.

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